FPIX - Electronics

Steve Schnetzer
Rutgers University

DOE/NSF Review

May 20, 2003

Overview

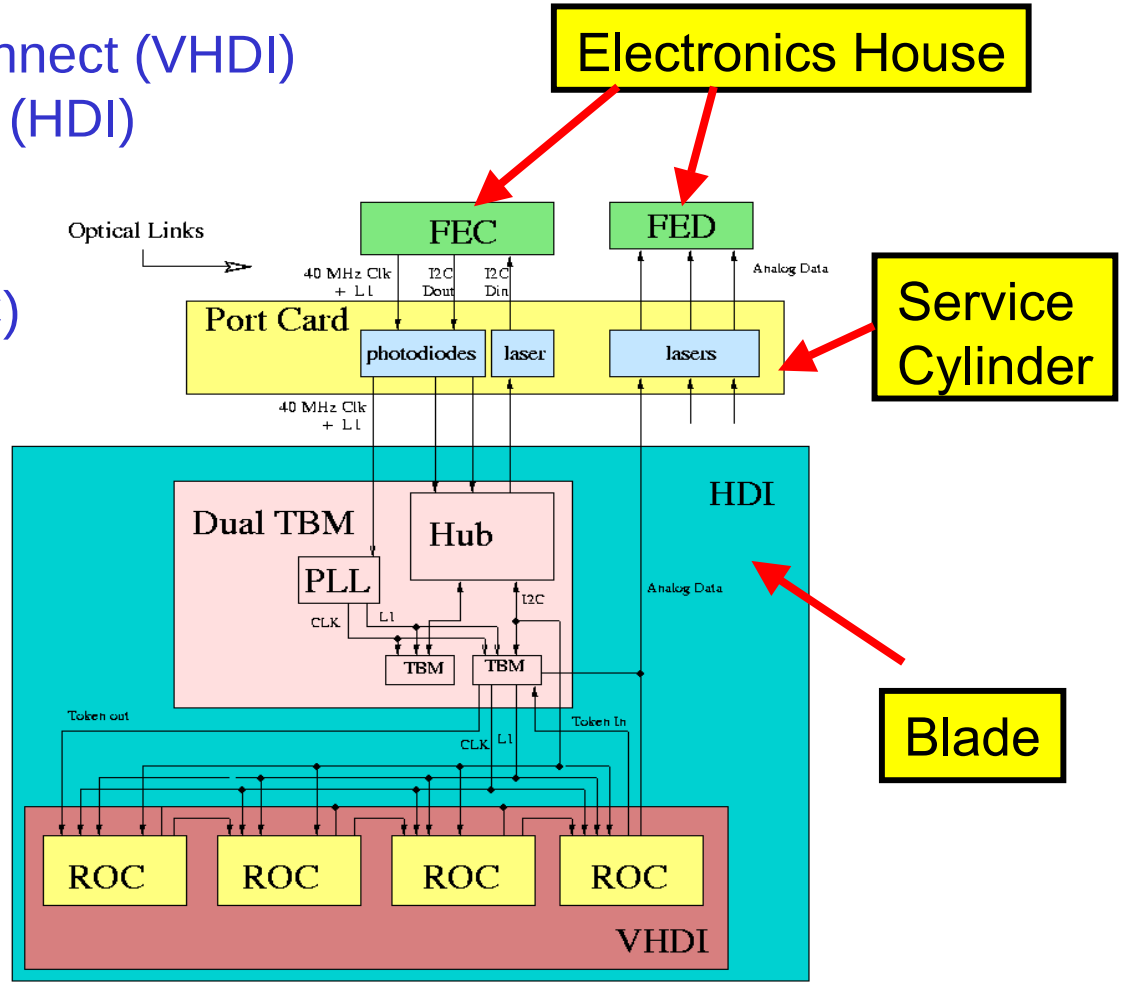
US CMS

- Very High Density Interconnect (VHDI)
- High Density Interconnect (HDI)
- Token Bit Manager (TBM)
- Port Card (and services)
- Front End Controller (FEC)

European Groups

- Readout Chip (ROC)
- Optical Links
- Front End Driver (FED)

System Tests



ROC

DSM translation of pixel Read Out Chip (ROC)

• Performance of present DMILL pixel read out chip under LHC equivalent rates tested at πM1 beam line at PSI. (Summer 2002)

– Efficiency measurements versus pion fluence (< 36 MHz/cm^2 track rate)
– 25nsec bunch crossing rate
– Continuous data taking and simultaneous readout operation

Result: Test very successfull ! No extra data loss mechanism seen !

• Translation of ROC into 0.25μ IBM techn. allows design changes due to :
  – more metal layers (5 instead of 2)
  – smaller feature size
  – higher speed
  – lower power (eventually also lower current)

• Translation into generic 0.25μm PSI rules started in Sept. 2002

Changes to ROC for 0.25μ translation

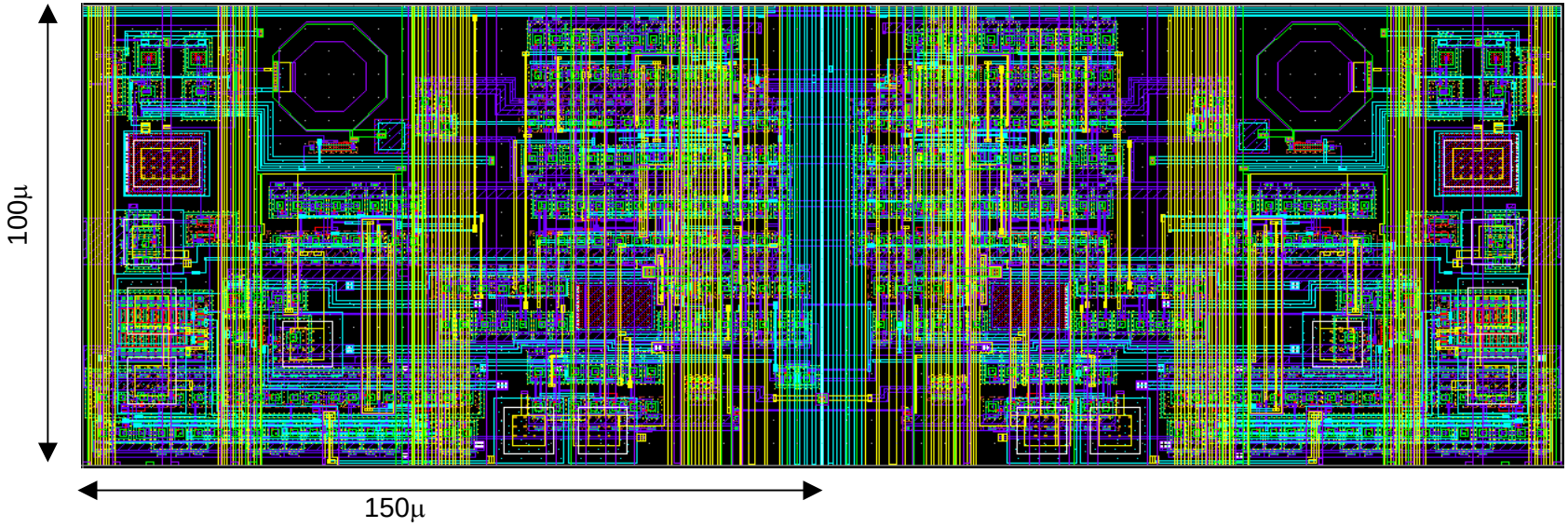
- pixel size: 150μ x 150μ → 100μ x 150μ
- number of pixels per double column: 106 pixel → 160 pixel

  → more address space required → new readout with 6 levels but still 6 clock cycles /pixel hit
- sensitive area almost unchanged 7800μ x 7950μ → 7800μ x 8000μ
- reduce periphery height : 2800μ → 1800μ
- changes to Column Drain Architecture (CDA):

  → remove insensitive "Load Cycle" for column scan
  → add 3rd hit capability during column scan
- change # of timestamp buffers and # of pixel hit data buffers
- changes in analog addressing mechanism (more reliable levels) → 1 fast DAC /chip
- change to positive supply voltage & reduce # of supply voltages (4 → 2)
- reduce analog & digital current consumption

Pixel Unit Cell of new deep submicron ROC

New pixel size 100µ x 150µ, back to back layout of double pixel, 5 metal layers



- full static logic.
- eliminate load cycle. (deadtime free CDA scanning)
- enable 3rd column hit. (2nd in DMILL ROC)
- 4 trim-bits for pixel threshold adjustment. (SEU improved)
- 9 bit internal binary address bus

Increase number transistors per pixel from 127 (old DMILL ROC) to 251 (new DSM ROC)

Size of Pixel Read Out Chip

- Present DMILL pixel readout chip has size (8 + 2.8) mm x 8mm

- Periphery of 2.8mm contains : timestamp buffers, pixel hit data buffers, control & interface block

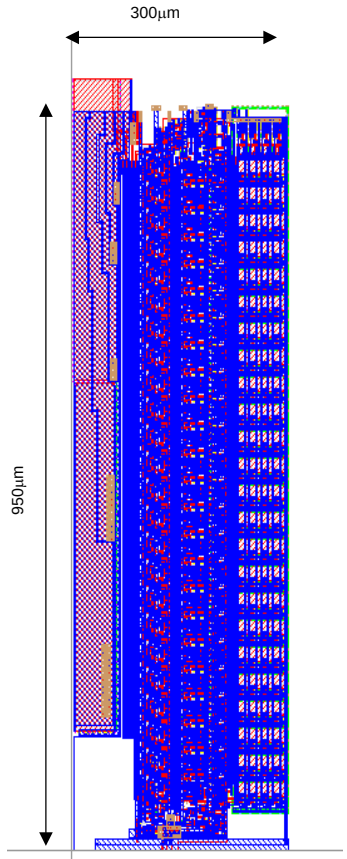
- For new 0.25µm ROC try to reduce size of periphery by 1000µm while increasing the number of timestamp (8→12) & data buffers (24→32).

- Simplifies construction for barrel modules

- More space for VHDI of forward pixel disks

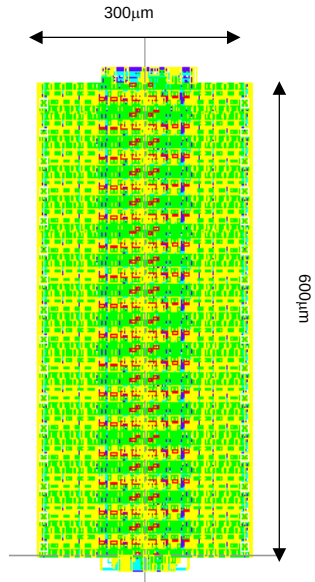
Data buffer cells for pixel hit storage

DMILL



• 24 pixel hits/DC

0.25µ IBM



New Data Buffer design done !

New ROC has more data buffer cells

• 32 pixel hits/DC

Data losses of pixel ROC

- Original ROC design (TDR) was done for high lumi operation of **7cm** layer!
- Use 0.25μ ROC translation to optimize for **new pixel size** and **4cm** radius !!

Data losses @ r=4cm & L=10^{34}	**DMILL ROC** DM_PSI43 150μ x 150μ pixel	**0.25μm ROC** IBM_PSI46 100μ x 150μ pixel	Status of translation
Timestamp (# buffers)	3.1% (8)	0.17% (12)	done
Data Buffers (# buffers)	0.1% (24)	0.15% (32)	done
Column Drain load cycle	3%	0%	done
Column Drain 3rd hit capability	1.4%	0.25%	done
Pixel overwrite	0.3%	0.21%	no change

Parameters of new DSM Pixel Read Out Chip

- Chipname: IBM_PSI46
- CMOS technology: IBM 0.25μm, bulk, 5 Metals (old **DMILL_PSI43**: 0.8μ BiCMOS, SOI, 2 Met)
- Size of final ROC layout: 7900 μ x 9800 μ (old **DMILL_PSI43**: 7950μ x 10800μ)
- 52 x 80 pixel = 4160 pixel (old **DMILL_PSI43**: 52x53 pixel = 2756 pixel)
- Pixel size (rφ x z) : 100 μm x 150 μm (old **DMILL_PSI43**: 150m x 150m)
- Number of transistors: 1280 K (old **DMILL_PSI43**: 430 K)
- Number of supply pads : 35 pads (175μ pitch) (old **DMILL_PSI43**: 42 pads of 150μ pitch)
- Number of external capacitors: 2 (old **DMILL_PSI43**: 6)
- Number of supply voltages: 2 (2.5V,1.75V) (old **DMILL_PSI43**: 4 (5V, 3.5V, 3V, 2.5V))
- Total supply current: estim. ~ 70 mA (old **DMILL_PSI43**: 160 mA)

Status of ROC translation (May 03)

- **Pixel matrix & readout**

Functional Block		Status / Date
data buffers		done / Okt. 02
timestamp buffers		done / Nov. 02
new column drain mechanism		done / Jan. 03
analog block & comparator	(tested in IBM_PSI44)	done / April 02
new analog addressing mechanism		done / Febr. 03
new readout mechanism		done / March 03
PUC (layout)		done / Jan. 03

- **Control & Interface Block:**

Functional Block		Status
I2C block		done / Feb 03
timestamp counters		done / Jan 02
DAC's		done / March 03
LVDS (low power)	(new)	done / April 03
Voltage regulators	(tested in IBM_PSI44 but needed more work)	done / April 03

- Assembly of complete ROC. Status: **Finished & send to CERN for checking** (16.5.03)

- Tape out of engineering run delayed by ~3 month to original planning.

PSI43 chip testing at FNAL

PSI43 wafer test stand designed and built

- Based on EED ASIC Test System and Cascade/Alessi 6171 semi-automatic

  8 inch chuck probe station

  - » Allows manual and semi-automatic testing of single chips and wafer

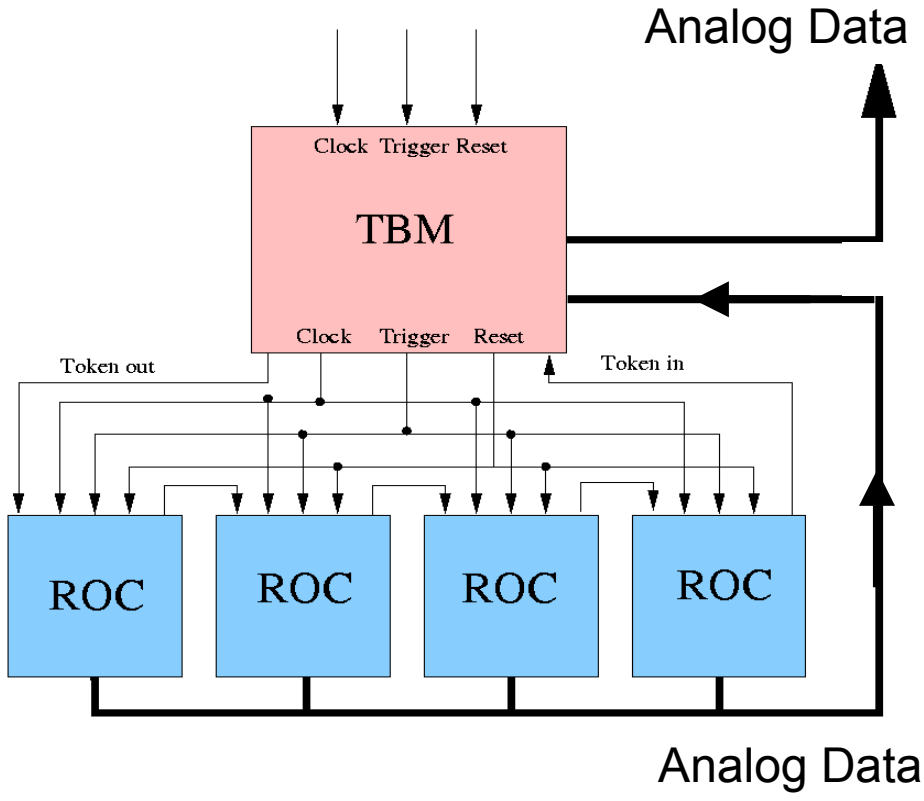
Results of PSI43 Testing at FNAL

- "Working" chip definition:
  - Currents and voltages are within expected range
  - Responded to the serial control interface commands (Last programmed DAC value changing)
  - Two or more (out of 26) double columns responded to the calibration trigger sequence
- ROC chip test results:
  - Tested several varieties of the chip:
    - » 31 chips on wafer, yield ~ 42%
    - » 31 diced chips, yield ~ 45%
    - » 17 diced and bumped chips, yield ~ 59%
    - » 71 bumped chips on wafer, yield ~ 37%
  - Overall yield of "working" chips (ignoring some pixel cell and double column defects) is ~ 46%

TBM

TBM Functions

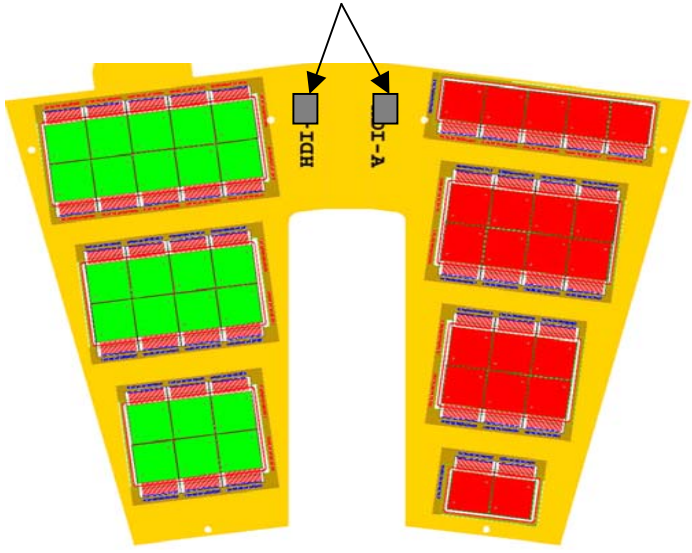
- Control readout through token pass
- Write header and trailer (Analog)
  - trigger #
  - error status word
- Distribute to ROC's
  - L1 triggers
  - clock
  - reset
- Stack triggers awaiting token pass
  - 32 deep
  - no readout after 16 deep
- Provide driver for analog signals

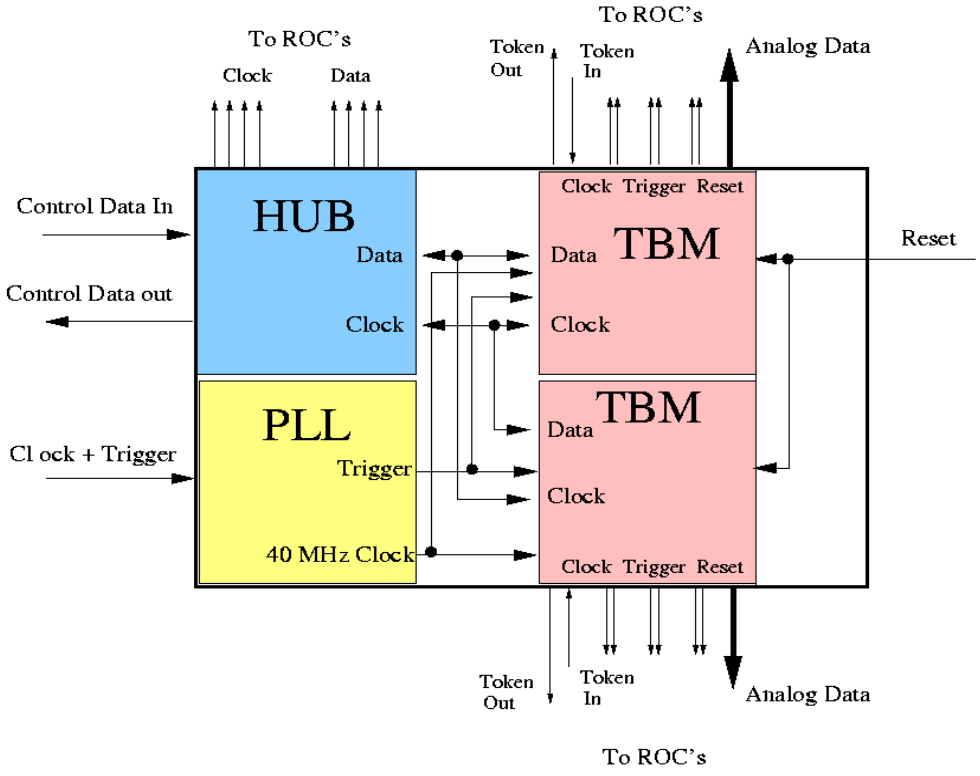


TBM Implementation

Dual TBM Chip

- Twin TBM's
  - two readouts for inner barrel layer
- Control Network Hub
  - port addressing for control commands
- 4-fold fanout (clock, trigger, reset)
  - LVDS drivers
- Located on porch of each side of blade

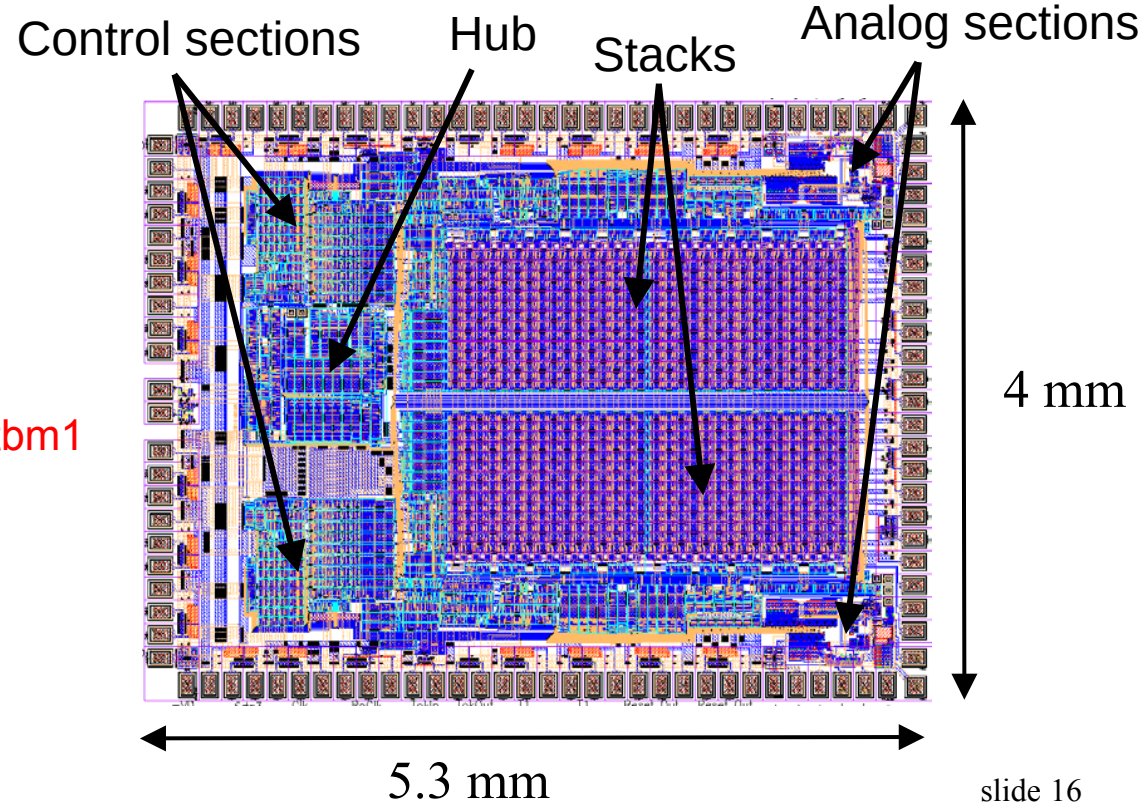




DMILL Dual TBM

Delivered
May '02

Fully functional at
full 40 MHz readout



For details see Ed Bartz's slides
and paper from Pixel 2002 at
www.physics.rutgers.edu/~bartz/cms/tbm1

DMILL TBM Test Results

- Header marker 3 “UBLK” + “1”
  - –8 Bit Event Number (4 Clocks)
- Trailer marker 2 “UBLK” + 2 “1”
  - –8 Bit Status Word (4 Clocks)

- Power consumption 600 mW
  - –core 140 mW
  - –Differential Drivers 460 mW
- 6 Tested / 5 Fully Functional

Translation to 0.25 Micron

Started Dec '02

Ed Bartz
Lalith Perera

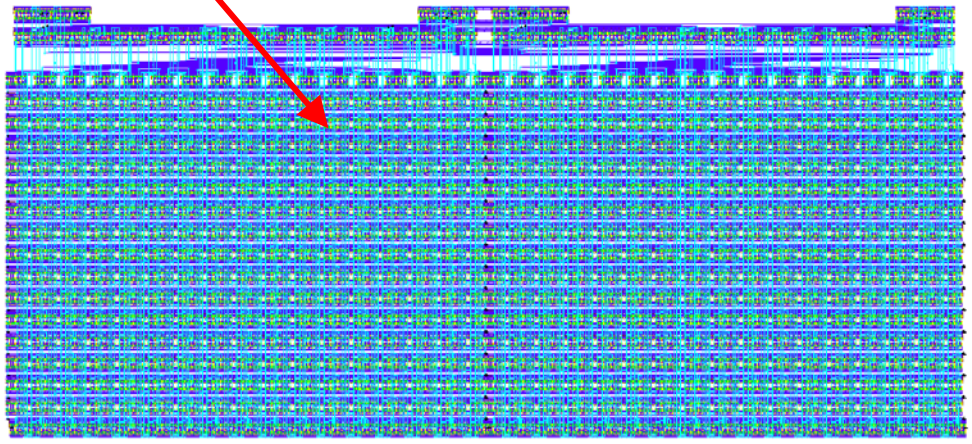
Completed to Date

Schematic: major blocks

Simulation: digital (Verilog) level
transistor level (HUB block)

Layout: 75% of HUB block
100% of stack block

Stack



HUB

TBM Modifications

- Eliminate PLL
  - PLL's will be located on service cylinder
  - separate clock and trigger lines will be sent over pigtails
- Incorporate line driver for analog signal
  - only one driver connected to long (50 cm) line
- LVDS drivers with lower voltage swings
  - Roland personally taking charge of this
- Lower power consumption of core
  - DMILL TBM was over designed
  - assumed too high internal capacitive loads
  - shut down clock when circuit not is use
- Increase pad pitch from 6 to 8 mils
  - easier HDI design

TBM Schedule/Resources

Schedule

First prototype submission	June ‘03
Second prototype submission	October ‘03
Final TBM available	End of ‘03

Resources

Ed Bartz (Rutgers Engineer)

Lalith Perera (Rutgers RA)

Assistance from PSI

TBM Concerns

⇒ Submission of “full” TBM in June ambitious

- if first “full” TBM submission by October
  → “full” TBM still be available by end of year

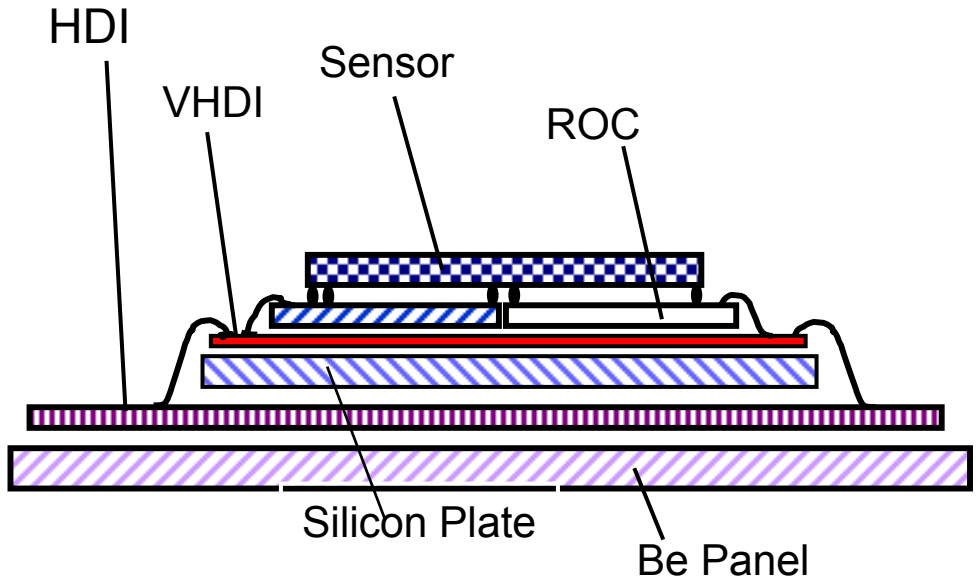
⇒ Schedule of fall CERN MPW submission

- MPW scheduled only if there is enough interest

VHDI

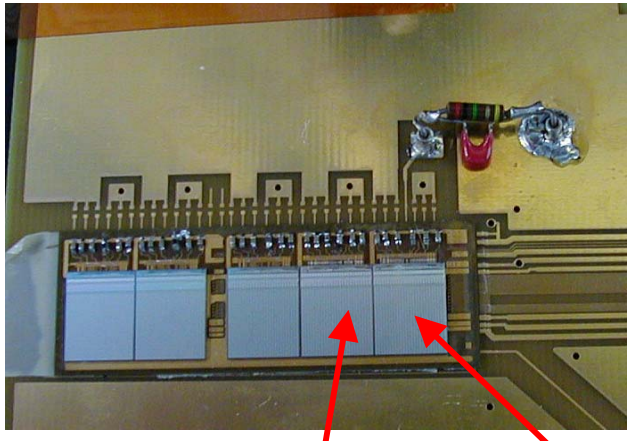
VHDI

- Circuitry for connecting ROC's on a plaquette
  - modularity
    - plaquette tested before mounting on blade
  - very high density
    - need to match 6 mil ROC pitch
  - two layer circuit
  - five sizes
    - 1x2, 1x5, 2x3, 2x4, 2x5
- Qualification of vendor
  - delivered Feb. '01
  - met specs
  - yield 50%
    - precision of via drill hole
      - ⇒ laser drilling

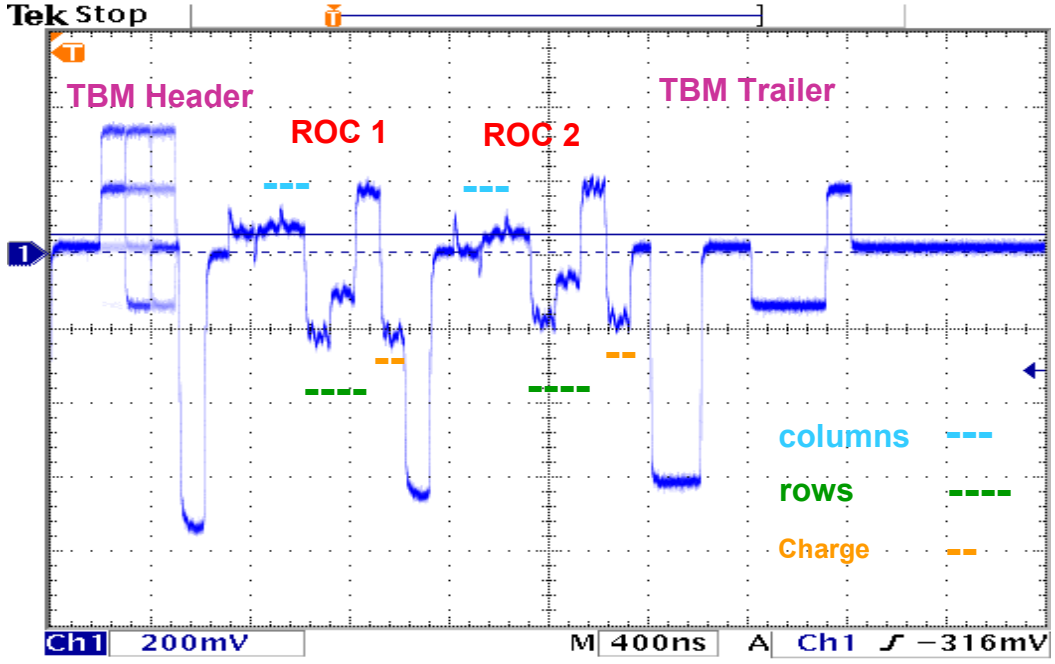


Test of 1 x 5 VHDI

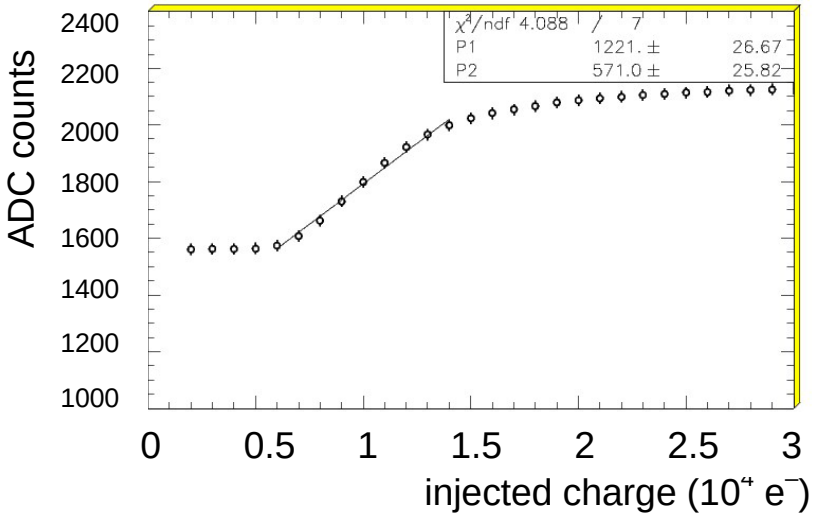
measure noise as one chip at a time is added to 1 x 5 VHDI



ROC's 1 & 2 on a 1x5 VHDI
Pulse Pixel in col 6, row 9



Calibration Curve



- noise level 150 to 200 electrons per channel
- slight increase in noise with addition of chips
- no large increase in noise or oscillation

Noise vs. number of ROC's

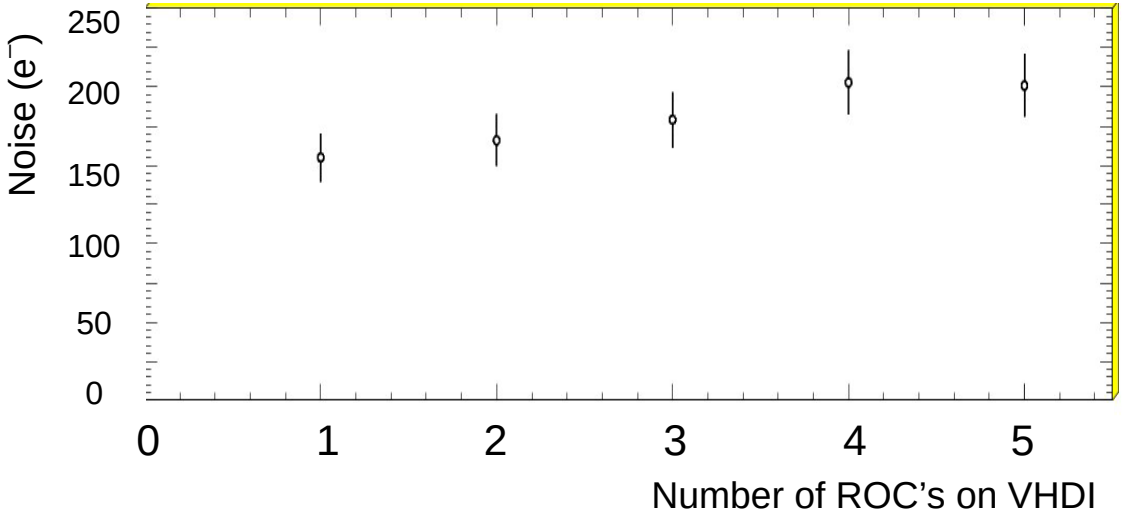


Table of noise in the various readout chips as a function of the number of the chips on the VHDL.

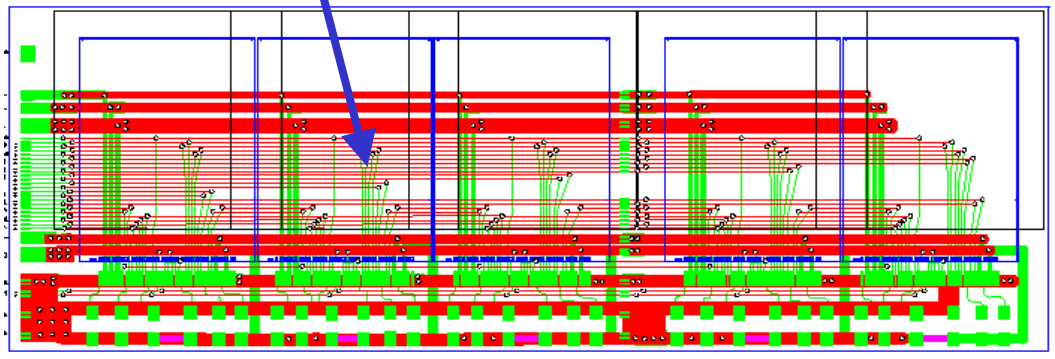
	number of chips on Plaquette (VHDL)				
	1	2	3	4	5
Roc 0	155	166	179	203	201
Roc 1		132	146	144	191
Roc 2			137	162	162
Roc 3				164	166
Roc 4					150

decreasing noise with increasing ROC number

may indicate pickup from fast trigger lines (lines were unterminated)

repeat measurement with fast trigger lines terminated

Fast trigger out lines



ROC 0 ROC 1 ROC 2 ROC 3 ROC 4

VHDI Schedule/Resources

Schedule

- Complete testing of populated 1x5 and 2x5 DMILL VHDI's — June '03
- Test VHDI with sensor mounted to ROC's — Aug '03
  determine requirements for filtering of bias voltage
- Design VHDI for 0.25 μm chips — Sep '03

Resources

- Testing of DMILL VHDI
  Bob Stone (Rutgers Physicist)
  Lalith Perera (Rutgers RA)
  Umesh Joshi (Fermilab Physicist)
- Design of 0.25 μm VHDI
  Mike Matulik (Fermilab Engineer)

VHDI Concerns

$\Rightarrow$ Need to start on 0.25 μm design soon to be ready for chips in the fall

HDI

HDI

- 2 - layer flex circuit
  - uses standard technology
- Covers both sides of blade
  - folded at edge in butterfly fashion
- Connects VHDI's to Dual TBM's
  - porch for mounting TBM
- Single pig tail
  - connects to Port Card
    - carries signals and power to and from blade

HDI Schedule/Resources

Schedule

- Submit prototype by end of year

Resources

- Design of HDI
  Mike Matulik (Fermilab Engineer)

HDI Concerns

⇒ Need HDI by Spring ’04 for blade tests

⇒ Some resource conflict with VHDI design

⇒ Important decisions to be made

- sensor bias voltage
  - how may separate voltages
  - how to bring in bias lines
    - separate lines or on pig tail
  - RC filters
    - how many and where
- fast trigger
  - is it implemented
    - what chips are needed

Control Network

FEC

Control Network

- Programming of front-end chips
  - ROC
    - pixel thresholds
    - trigger latency
    - set calibration mode
    - reset
  - TBM
    - enable/disable trigger/tokens
    - reset
  - Laser Driver
    - bias current

Three Components

- Front End Controller (FEC)
  - VME module
- High speed Hub
  - incorporated in Dual TBM chip
- Low speed Hub / Fan In/out

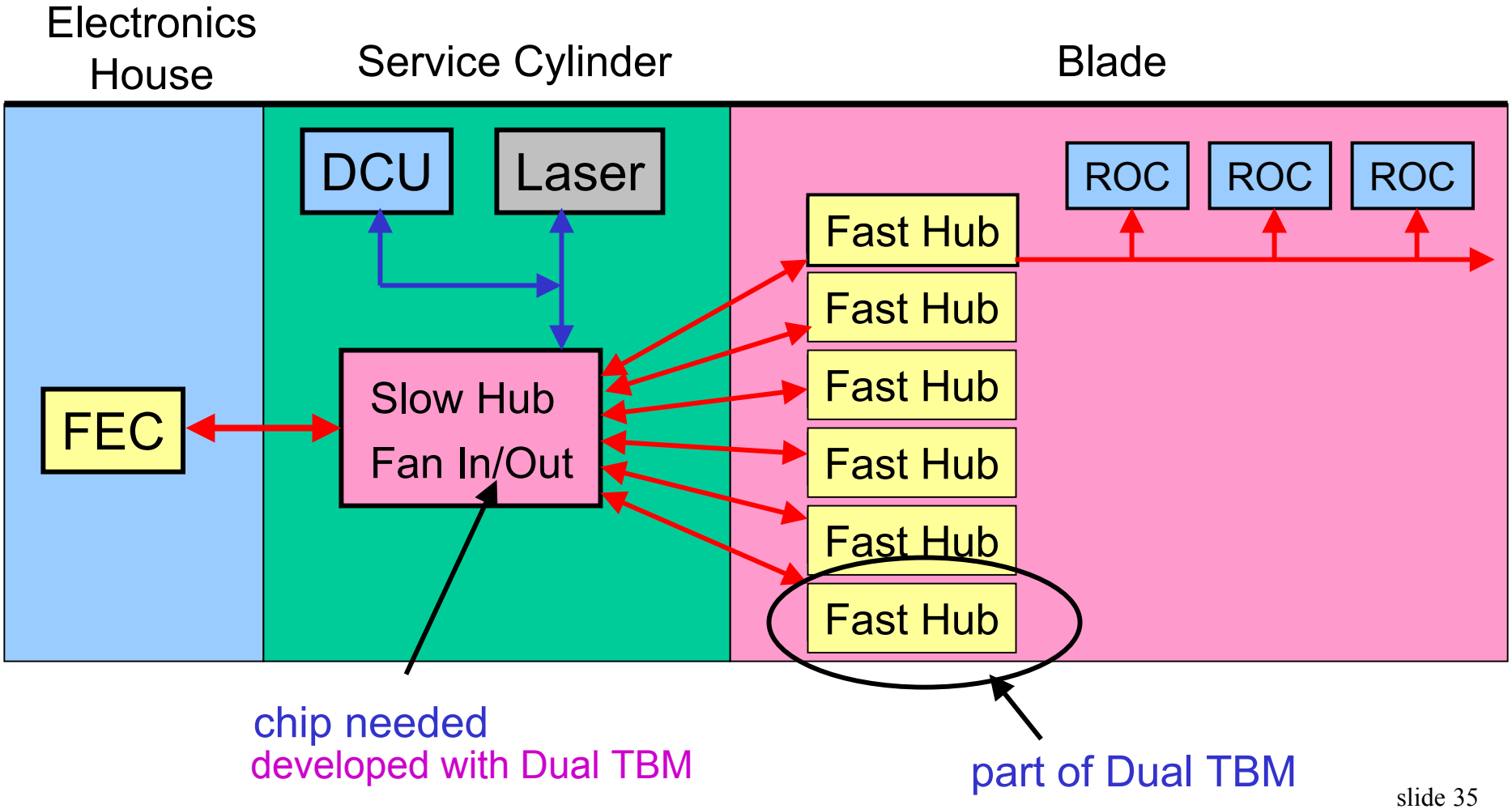
Single Event Upsets

→ reset pixel thresholds frequently

⇒ High Speed

run at 40 MHz

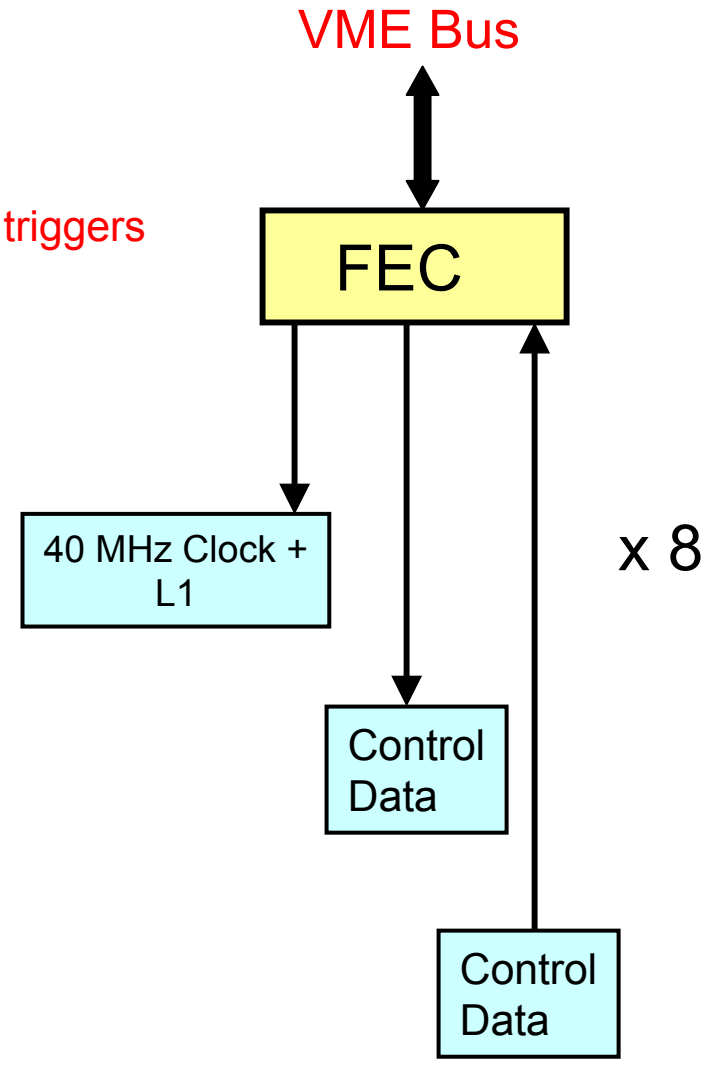
Control Network Link



Front End Controller

Gate array based VME module

- 8 channels (links) per module
- sends to front-end
  - 40 MHz LHC clock with embedded L1 triggers
  - control network data
- receives from front end
  - reflected back data
    - verifies that Hub was addressed
    - checks data integrity
    - clock/data phase adjustment
- uses I^2C start/stop protocol
- 64 Mbytes on-board memory
  - stores control commands
  - mostly pixel thresholds and addresses
- during “empty” orbit
  - control commands downloaded
    - 2 columns of thresholds @ 40 MHz



FEC Prototypes

Ed Bartz

4 stages of development

- parallel port version (exists)
  - downloading of commands through PC
- gate array version (Spring ’04)
  - blocks of commands stored locally
  - PC initiates sending of command blocks
  - “final” FEC front - end
- VME version (Spring ’05)
  - communication to FEC via VME
  - “final” FEC back - end
- Production version (Fall ’05)
  - full VME module

Tracker FEC

investigate whether we can use the tracker FEC

reprogram PGA for pixels

may save development time

Caveats

- much higher data through put than tracker
  - 3.5 kB per link during 88 μs empty orbit
- will need high speed PGA
- need 8 MB of memory per link
  - could download to FEC between empty orbit
    - 200 kB/s on VME bus

Port Card / Services

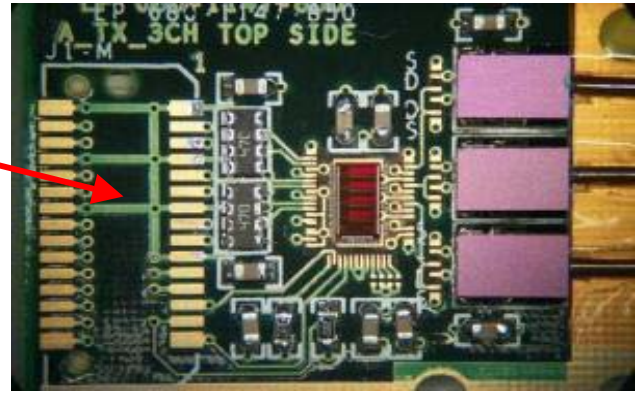
Port Card

since last review

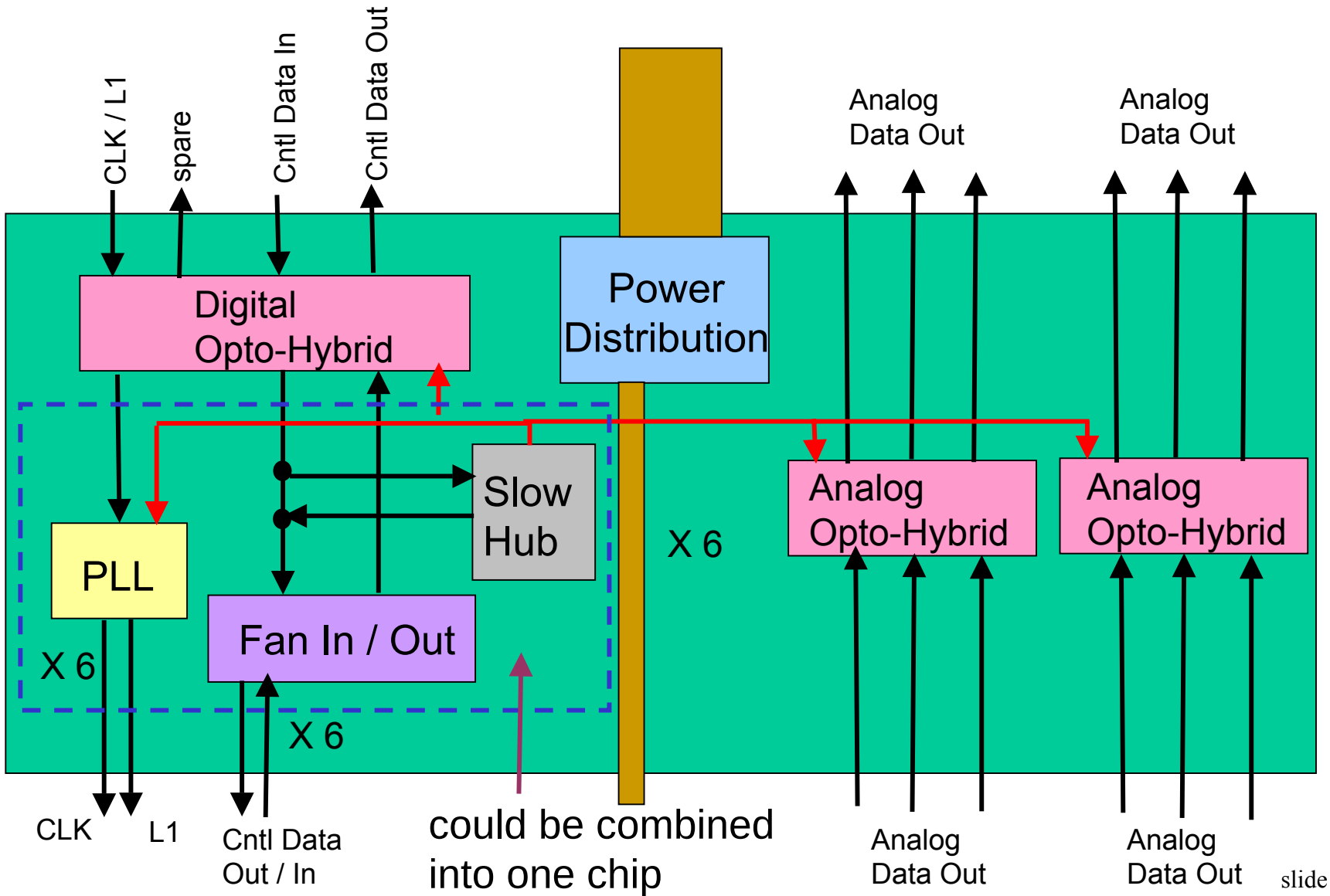
Port Card moved

detector → service cylinder

no space for opto-hybrid boards at detector



Port Card for 3 Blades



Port Card / Services Concerns

⇒ Need prototype by Spring ’05
for multiple blade tests
multi layer circuit board

Major Concern is for the associated services

- mounting of Port Cards
- cooling of Port Cards
- distribution of power
- cabling on service cylinder
- cabling between service cylinder and detector

need engineering resources

System Tests

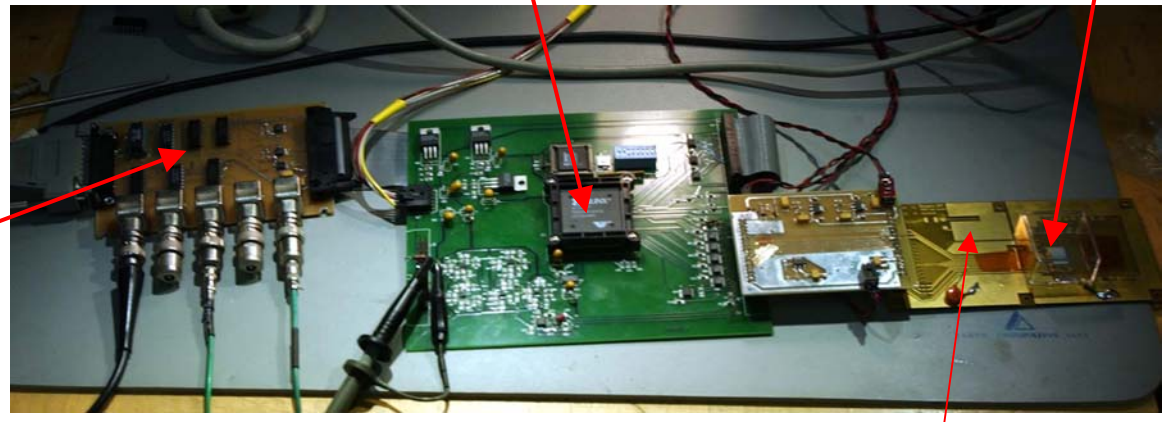
Bob Stone
Lalith Perera
John Doroshenko
Ed Bartz

Test Stand

ROC on VHDI successfully tested

FPGA TBM

VHDI with Readout Chip

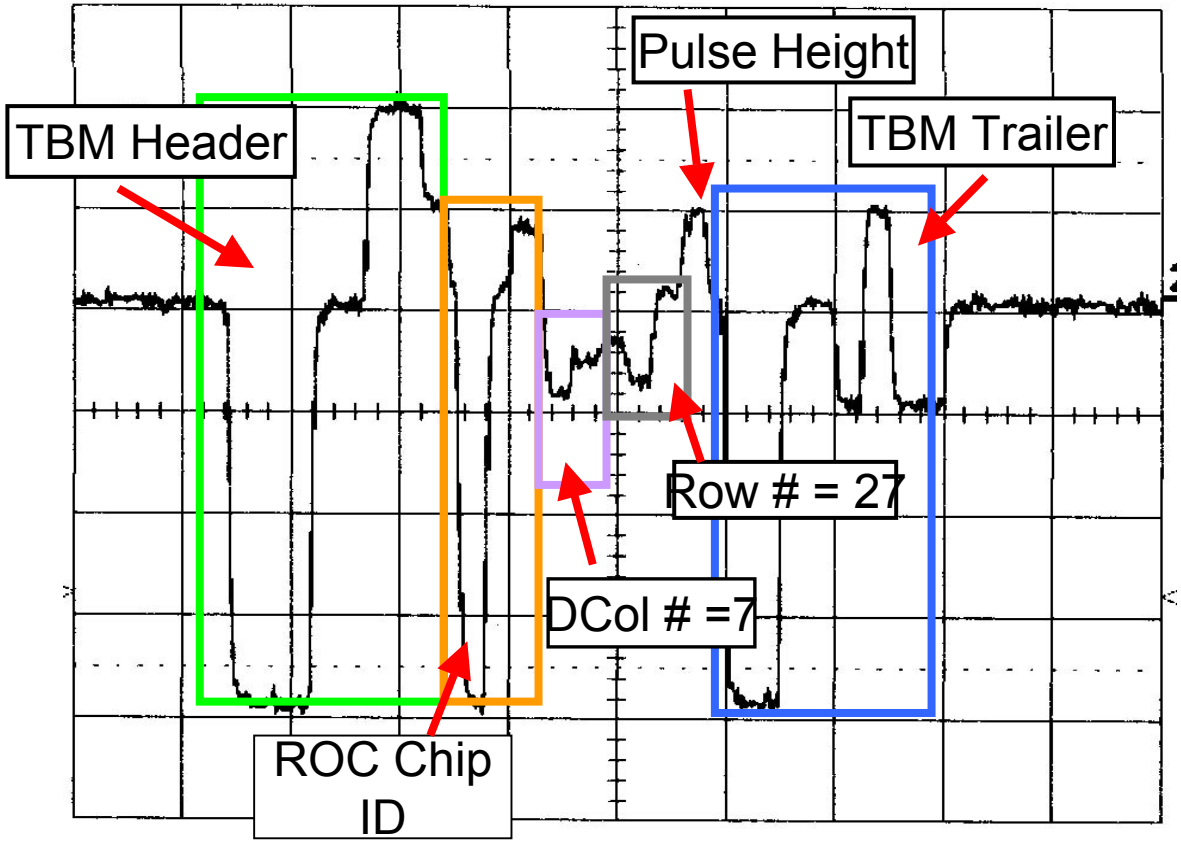


FEC Prototype 1

"HDI" board accommodates 1x1, 1x5 and 2x5 VHDI's

8 test stands produced

Test Stand Readout of ROC on VHDI



Test Stand Evolution

		Test
October '03	DMILL VHDI ⇒ 0.25 μm VHDI Incorporate 40 MHz ADC	⇒ Plaquettes
March '04	"HDI" board ⇒ prototype HDI PGA TBM ⇒ 0.25 μm TBM Upgrade to FEC (Version 2)	⇒ Panel
Oct '04	Upgrade to FEC (Version 3) Incorporate FED } VME	⇒ Blades
March '05	Incorporate Port Card Incorporate Optical Links } optical readout	⇒ Multiple Blades

parallel software development

Summary

Task	Schedule	Engineering Resources
ROC	0.25 μm ROC Fall '03	PSI, Baldin
TBM	production TBM Spring '04	Bartz, Perera
VHDI	0.25 μm VHDI Fall '03	Matulik
HDI	0.25 μm HDI Spring '04	Matulik
FEC	ready for production Fall '05	Bartz
Port Card	prototype Spring '05	Los
Services	lots of engineering design work needed now	Baldin, Los